INTERDATA

Digital Systems

Model 2

Model 3

Model 4

At last, a family of compatible low-cost digital systems.

Interdata has created a family of small to medium scale digital systems designed to provide the user with a choice of instruction execution time, memory size and speed, and instruction repertoire options, with low and high speed input-output channels. Software packages are designed to fit the capability of each computer. Programs are upward compatible between processors. Most important, all peripheral devices and system components are interchangeable between models.

Digital systems from Interdata are competitive with a broad range of complex logic systems and special purpose controllers. The user who has even the most sophisticated requirements is provided with system flexibility to solve a wide range of industrial control and scientific computational problems.

Interdata digital systems can be used for:

- Automatic test and inspection.
- Satellite data concentrator.
- Data acquisition and logging.
- Nuclear and medical measurement.
- Numeric control.
- Logic and switching systems for process control.

These third generation units have dual, in-line integrated circuits to provide excellent reliability. They are modular. Interdata systems furnish the user an expandable building block structure that can be adapted to a variety of system requirements. Standard off-the-shelf processors and memory modules, peripheral devices, system modules and components can easily be assembled into operational systems for specialized requirements.

Most significant, Interdata digital systems provide big machine processing capability at small machine cost. System features include:

A high speed, 16-bit halfword memory is addressable and alterable to the 8-bit byte level.

Memory is field expandable to 65,536 bytes. All memory is directly addressable with the primary instruction word, no paging or indirect addressing is required.

Sixteen general registers each 16-bits long can be used as index registers or accumulators.

Register-to-register instructions permit operations between the 16 general registers, eliminating redundant loads and stores.

A comprehensive instruction set includes efficient byte processing instructions, single instructions for loop control to increment-test-branch on index values, as well as instructions that test the condition code and branch directly to any location in memory.

Logical and arithmetic shift instructions can shift up to 15 positions with a single instruction.

Flexible, multiplexed input-output systems include an integrated priority interrupt facility and provide for direct addressing of up to 256 devices.

High speed memory access channels permit cycle stealing input/output to byte oriented peripherals or 16-bit halfword special purpose devices.

Third generation data compatibility includes ASCII and EBCDIC codes.

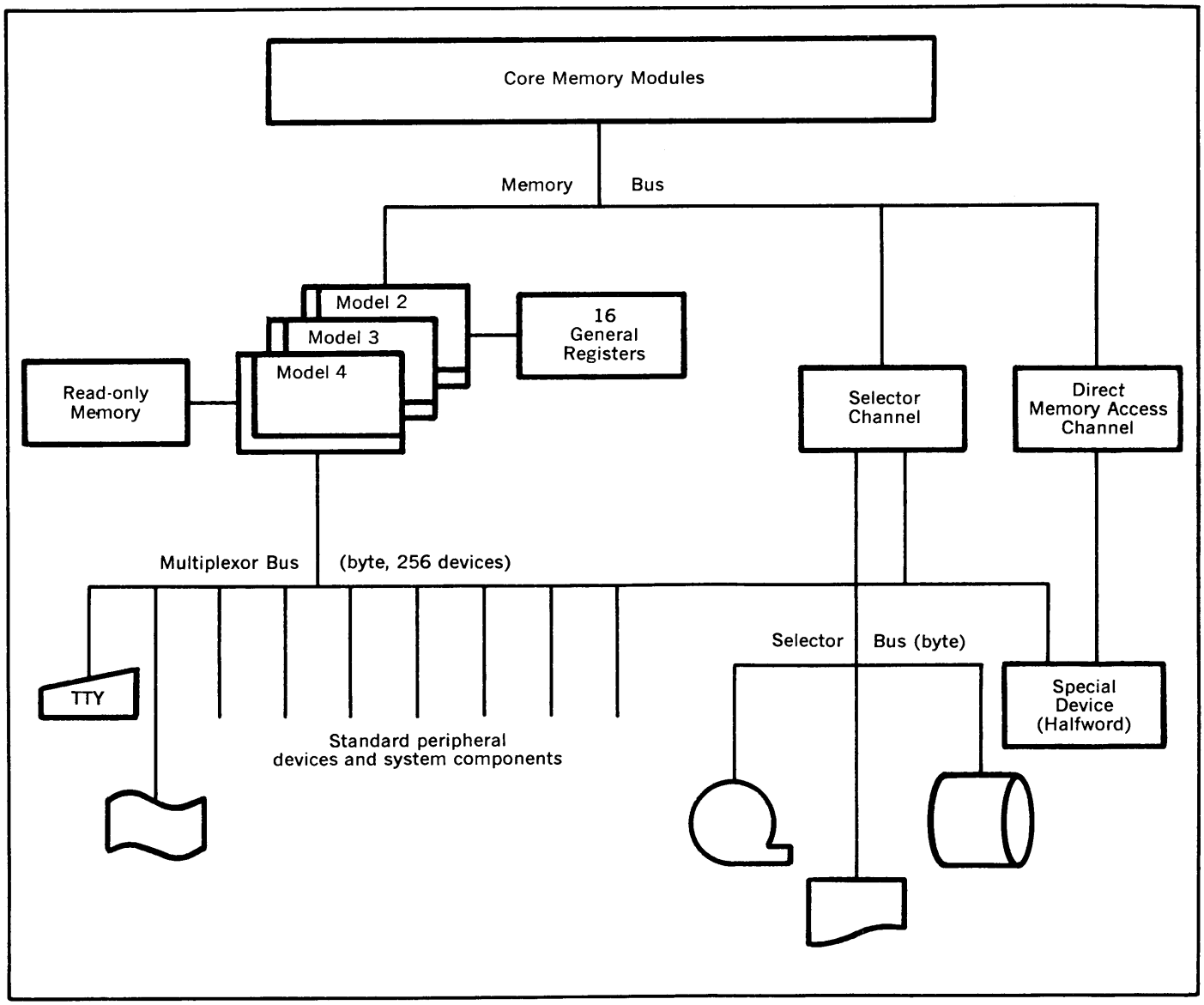
The comprehensive software packages include FORTRAN, Assembler, Debugging, Editor, Mathematical Library, and Input/Output system.

System architecture offers a high degree of flexibility.

Interdata computer systems are modularly structured to provide a high degree of flexibility in configuring application-oriented systems.

The "building blocks" used in the organization of Interdata systems include memories, processors, peripheral devices and system modules.

Here is the system block diagram.



Systems have modular memory to provide 8, 16 and 32 bit processing.

Interdata digital systems provide for connection of multiple memory modules on a memory bus to the processor. Field expansion of memory requires only plug-in of additional modules to a pre-wired chassis.

The memory elements of most Interdata systems can be expanded to a maximum dynamic addressing range of 65,536 bytes. An optional memory parity checking facility is available with a separate parity bit for each 8-bit byte. A memory parity error is serviced by an interrupt routine.

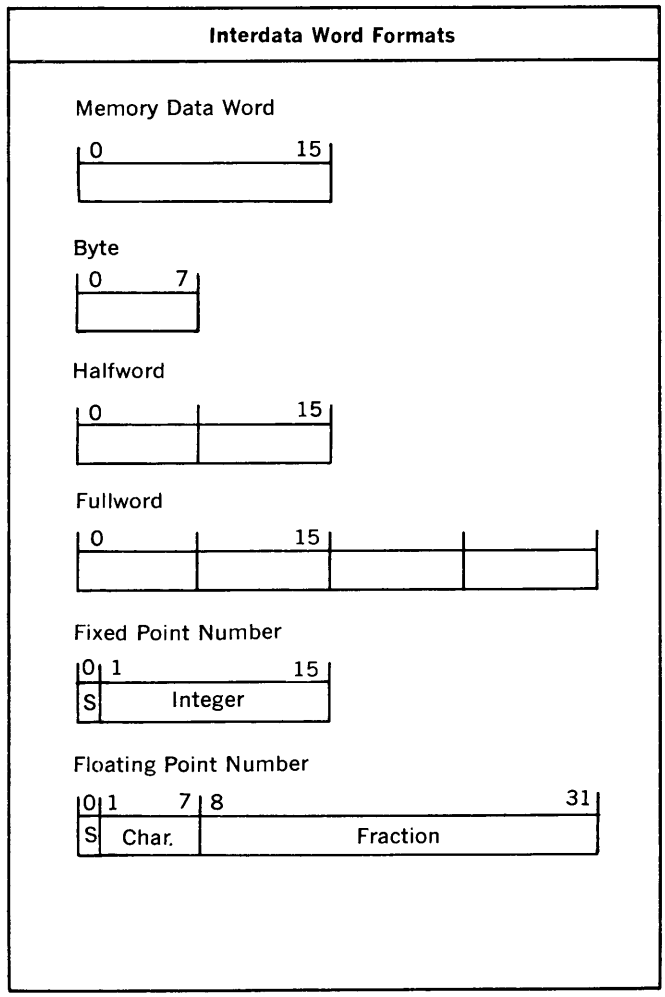
With a 16-bit halfword data register, all 16-bit instructions, fixed point data and logical data are handled in a single high speed memory cycle. Multiple halfword data requires one additional memory cycle for each 16-bit halfword. Byte operations are performed by the processor selectively manipulating the right or left 8 bits of the 16-bit halfword.

Processor is central building block.

The processor executes the instructions used in the application-oriented programs. Interdata processors are unique in providing a combination of hardware and firmware (Read-Only Memory) decoding of computer instructions. Hardware processors are selected for applications where speed of execution is an important factor; firmware processors provide greater economy at slower speeds without sacrificing flexibility. All processors include a 32-bit Program Status Word, four pair of 'old' and 'new' PSW's for interrupt servicing, a 32-bit Instruction/Address register, and sixteen General Registers.

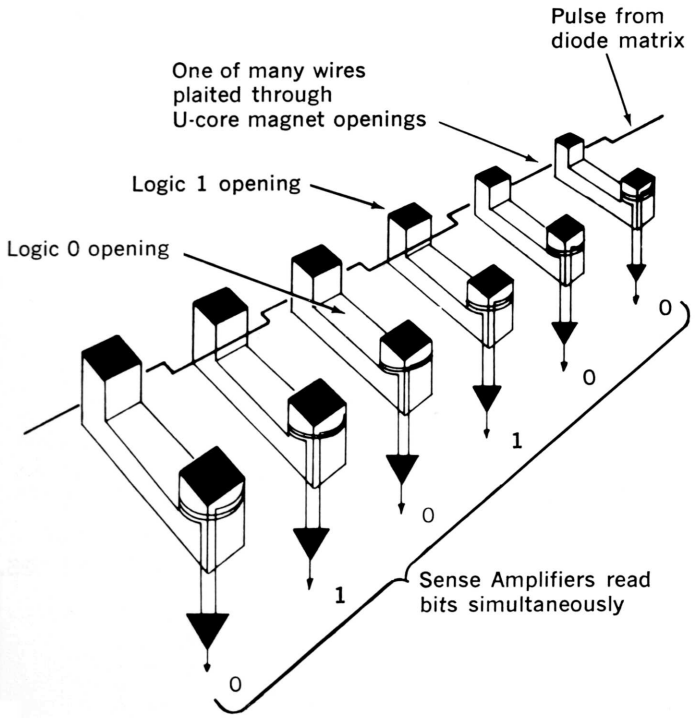
Each processor General Register contains a 16-bit halfword and can be used as an index register, a fixed point arithmetic accumulator, or as a logical accumulator. Processors with optional hardware floating point instructions contain an independent set of 32-bit floating point registers.

After execution of most instructions the status of the result is recorded in the condition code field of the Program Status Word. These condition codes indicate whether the result was greater than, equal to, or less than zero. Also indicated are carry/borrow and overflow conditions. This facility for automatically testing results and setting the appropriate condition codes saves numerous 'test and skip' instructions.



Read-only memory offers unique control.

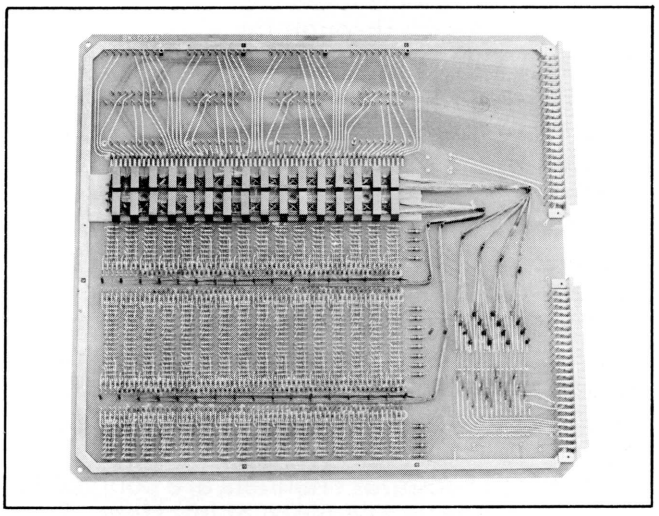
The ROM is a high speed (400 nanosecond) non-destructive memory which stores the micro-program used to interpret and execute the main program. The micro-program is hard-wired in an array of 16 pulse transformers. Each transformer represents one of 16 bits in the micro-instruction word. The "word lines" are threaded through the transformer array with one line for each 16-bit word. Passage of the line on either the inside or outside of the transformer is equivalent to storing a "1" or "0" respectively. In operation, a pulse driven down a selected "word line" produces the hardwired 16-bit word pattern on the bit lines.



"Firmware" micro-programs pre-wired into the ROM are coded in a manner similar to conventional programming. A typical group of micro-instructions to increment and test a 16-bit number is as follows:

```
AGN     L     AR,X'2'          LOAD 2 IN AR
        A     R2,R2,CO         ADD TO R2
        A     R1,R1,CI+NA      ADD WITH CARRY TO R1
        B     V,OVER           BRANCH ON OVERFLOW
        B     CGL,AGN          BRANCH TO AGN
```

The micro-program is contained on one or more special printed circuit boards. The entire instruction repertoire of an Interdata system can be changed by substituting pre-wired circuit boards, or special instructions can be added to the standard repertoire. With this capability, Interdata can provide custom repertoires to meet special requirements in application oriented systems.



Partially Wired Read-Only Memory Board

Input/output structure handles a wide range of system requirements.

The input/output structure provides three different channels for handling data in the system. They are the

Multiplexor Channel
Selector Channel
Direct Memory Access Channel

The Multiplexor Channel transfers byte oriented data under program control between the processor and an active device. Either single bytes or a block of bytes can be transferred depending on the instruction used. In either case, the processor is committed to servicing the device until the transfer is complete. Under program interrupt control a number of low speed devices can be operational at the same time.

The Selector Channel provides high speed, byte oriented data transfer between memory and an active device. Up to twenty-five devices can be connected to a single channel. The Selector Channel is initialized for block transfer by the processor through the Multiplexor Channel. Once initialized, the Selector Channel handles data transfer independent of the processor thereby freeing it for other work.

The Direct Memory Access Channel (DMAC) is a high speed, 16-bit data path between memory and a special purpose device. The connected device operates directly into the memory by establishing the appropriate address and executing Read or Write cycles. Data is transferred directly onto the memory bus at the selected address. Therefore, the DMAC does not require any processor operating time.

The input/output channels are coupled to the processor by two types of interface. The Multiplexor and Selector Channels use a byte oriented interface while the Direct Memory Access Channel uses a 16-bit interface as indicated in the diagrams.

The Multiplexor/Selector Channel Interface is the "standard" interface for connecting all peripheral devices and system modules. This interface contains two 8-bit registers called System Control and System Data, in addition to the Synchronize and Attention control lines.

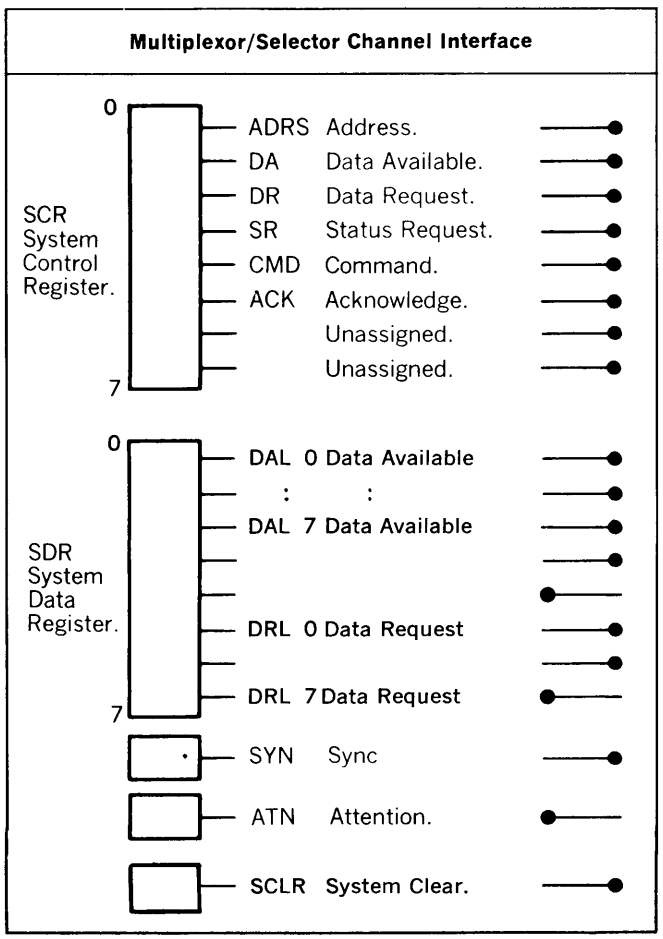
The bits of the System Control Register are used to define the type of data present on the data lines, i.e., if the address bit is high, the information on the data lines is a device or module address. Data is transferred from the processor to the device with the Data Available control and from the device to the processor with the Data Request control. In both directions the data is fully buffered. The Sync line is used as the master control line for executing request/response/release type signal interlocking.

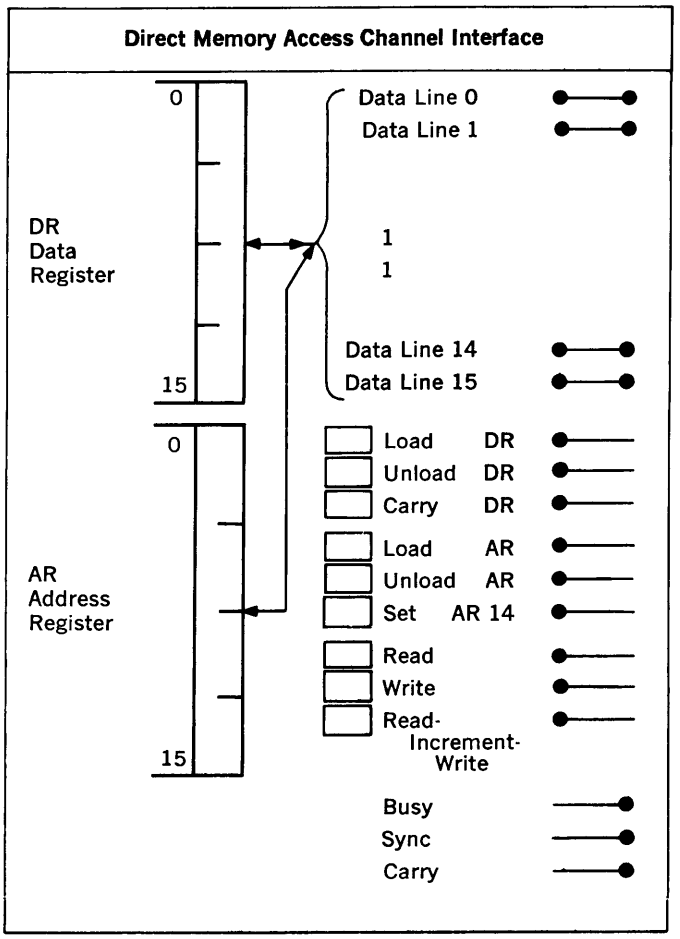
Attention (ATN) is a common line which the devices use to interrupt the processor. The interrupt Acknowledge (ACK) line is coupled through each of the attached devices and modules to form the system interrupt facility. The acknowledge signal originates in the processor.

Priority is determined by physical position on the interrupt chain with the device or module logically closest to the processor having the highest priority. To determine the highest priority device or module requesting an interrupt, the Acknowledge control line is raised. As this control signal is coupled through the attached devices, the highest priority device on the chain will place its address on the data lines.

This Systems Interface is an easily-understood yet comprehensive facility for interfacing a wide range of devices, modules or other special attachments. The interrupt organization permits the individual and unique identification of up to 256 devices, modules or signals in a hardware priority structure with overriding enable/disable facilities. The Sync system eliminates the requirement for intricate timing and furnishes the positive interlocks required to match the wide range of asynchronous devices and modules connected to the interface.

The Direct Memory Access Channel Interface is a "special" interface for connecting single devices requiring a high speed, 16-bit data path to memory. This interface contains two 16-bit registers called Data and Address in addition to a number of command and control lines. The detailed operating characteristics of the interface structure are outlined in the Input/Output System Manual.

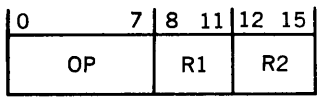




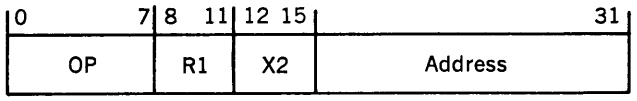
Interdata systems have third generation instruction format.

The system has three instruction formats. The 16-bit halfword instructions are the RR format. The 32-bit fullword instructions are RX or RS format.

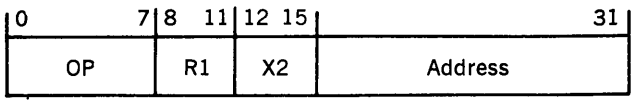
RR format:



RX format.



RS format:



The 4-bit and X fields each specify 1 of the 16 general registers. Each of the 16 halfword general registers can be used as an index register, as a fixed point arithmetic accumulator, or as a logical accumulator.

The RR instructions are for operations between the general registers. The R1 and R2 fields specify the first and second operands respectively. For a register-to-register Add operation [(R1)+(R2)⟶(R1)].

The RX instructions are for operations between the general registers and memory. The R1 field specifies the first operand and the X2 and Address field specify the second operand. For a register-to-indexed memory Add operation [(R1)+(Address+(X2)⟶(R1)].

The RS instructions are for shifting and branching. Operations involving immediate operands also use the RS format. For the immediate instruction the R1 field specifies the first operand and the sum of the contents of the X2 and Address field form the second operand. For an Add immediate operation [(R1)+Address+(X2)⟶(R1)]. The shift count is given by |Address+(X2)]

Instruction alignment.

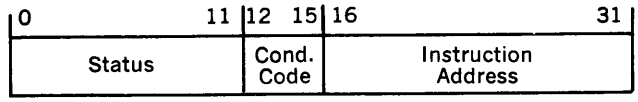
Halfword RR format instructions and fullword RX and RS format instructions are aligned on halfword boundaries. This permits mixing of halfword and fullword instructions with no requirement for halfword NO-OP's to force correct fullword instruction memory alignment.

Addressing.

The entire 65,536 bytes of core memory can be directly addressed by the primary instruction word. No indirect addressing or paging is required.

Program Status Word.

The status of the machine is defined by the program status word. It contains the Status, Condition Code, and Instruction Address.



Status Bit.	0	Wait State
	1	I/O Interrupt Enable
	2	Machine Malfunction Interrupt Enable
	3	Arithmetic Fault Interrupt Enable
	4-11	Undefined
		Arithmetic/logical
Condition Code Bit.	12	C—Carry/Borrow
	13	V—Overflow
	14	G—Greater than Zero
	15	L—Less than Zero
		Input/Output
	12	BSY—Device busy
	13	EX—Examine status
	14	EOM—End of media
	15	DU—Device unavailable

A powerful instruction repertoire with expansion options.

The basic repertoire of instructions is available in all Interdata computing systems. Hardware multiply and divide, block transfer, and floating point instructions are optional on some models.

Instruction set:

Type	Operation	Mnemonic	Format
Load and Store Instructions	Load Halfword	**LHR**	RR
		LH	RX
		LHI	RS
	Store Halfword	**STH**	RX
	Load Byte	**LBR**	RR
		LB	
	Store Byte	**STBR**	RR
		STB	RX
	Load Program Status Word	**LPSW**	RX
Fixed Point Arithmetic Instructions	Add	**AHR**	RR
		AH	RX
		AHI	RS
	Add with Carry	**ACHR**	RR
		ACH	RX
	Subtract	**SHR**	RR
		SH	RX
		SHI	RS
	Subtract with Carry	**SCHR**	RR
		SCH	RX
	Multiply (optional)	**MHR**	RR
		MH	RX
	Divide (optional)	**DHR**	RR
		DH	RX
Floating Point Arithmetic Instructions (optional)	Add	**AE**	RX
	Subtract	**SE**	RX
	Multiply	**ME**	RX
	Divide	**DE**	RX
	Load	**LE**	RX
	Store	**STE**	RX
	Compare	**CE**	RX
Logical Instructions	AND	**NHR**	RR
		NH	RX
		NHI	RS
	OR	**OHR**	RR
		OH	RX
		OHI	RS
	Exclusive OR	**XHR**	RR
		XH	RX
		XHI	RS

Type	Operation	Mnemonic	Format
	Compare Logical	**CLHR**	RR
		CLH	RX
		CLHI	RS
Shift Instructions	Shift Left Arithmetic	**SLHA**	RS
	Shift Right Arithmetic	**SRHA**	RS
	Shift Left Logical	**SLHL**	RS
	Shift Right Logical	**SRHL**	RS
Branch Instructions	Branch And Link	**BALR**	RR
		BAL	RX
	Branch on False Condition	**BFCR**	RR
		BFC	RX
	Branch on True Condition	**BTCR**	RR
		BTC	RX
	Branch on Index Low or Equal	**BXLE**	RS
	Branch Unconditional	**BR**	RR
		B	RX
	Branch on Zero	**BZ**	RX
	Branch on Not Zero	**BNZ**	RX
	Branch on Plus	**BP**	RX
	Branch on Not Plus	**BNP**	RX
	Branch on Minus	**BM**	RX
	Branch on Not Minus	**BNM**	RX
	Branch on Carry	**BC**	RX
	Branch on Overflow	**BO**	RX
	Branch on Low	**BL**	RX
	Branch on Not Low	**BNL**	RX
	Branch on Equal	**BE**	RX
	No Operation	**NOPR**	RR
		NOP	RX
Input/output Instructions	Read Data	**RDR**	RR
		RD	RX
	Write Data	**WDR**	RR
		WD	RX
	Read Block (optional)	**RBR**	RR
		RB	RX
	Write Block (optional)	**WBR**	RR
		WB	RX
	Acknowledge Interrupt	**AIR**	RR
		AI	RX
	Sense Status	**SSR**	RR
		SS	RX
	Output Command	**OCR**	RR
		OC	RX

Software packages to fit system requirements.

Interdata computing systems are supported by these software packages designed to meet user application needs:

- FORTRAN
- Assembler
- Debug
- Editor
- Math Library
- Input/Output System

Interdata FORTRAN is an interactive system with program statements entered on the teletype and executed immediately. This on-line system needs no program preparation other than entry of the source information. Program corrections can be made while the programs remain in core; the tedium of compiling and loading the object program is eliminated.

The Assembler translates symbolic source statements into a binary object program. The object program can be in a relocatable, linking loader format or absolute binary. Extensive pseudo ops include ENTRY and EXTRN that permit separate assemblies to be linked together at load time by the linking loader.

Debug is designed for efficient, on-line, interactive debugging.

Features available to the user are:

- Examine and modify a memory cell
- Address arithmetic
- Relative addressing of memory
- Multiple break points
- Search on limits for masked value
- Print or punch content of memory
- Execute the user program
- Register examination

The Editor is a system for generating source program paper tapes for the Assembler. The source program is entered from a teletype keyboard and stored in memory. The current line can be corrected, deleted, or changed and the entire program listed before punching a source tape.

A complete math library of function routines in fixed and floating point are provided with Interdata systems. These include:

- Binary to decimal conversion
- Decimal to binary conversion
- Multiply
- Divide
- Square Root
- Logarithm
- Exponential
- Arctangent
- Sine
- Cosine

Input/Output system provides driver packages for peripheral devices and system modules in addition to media conversion utility routines.

I/O Driver Packages

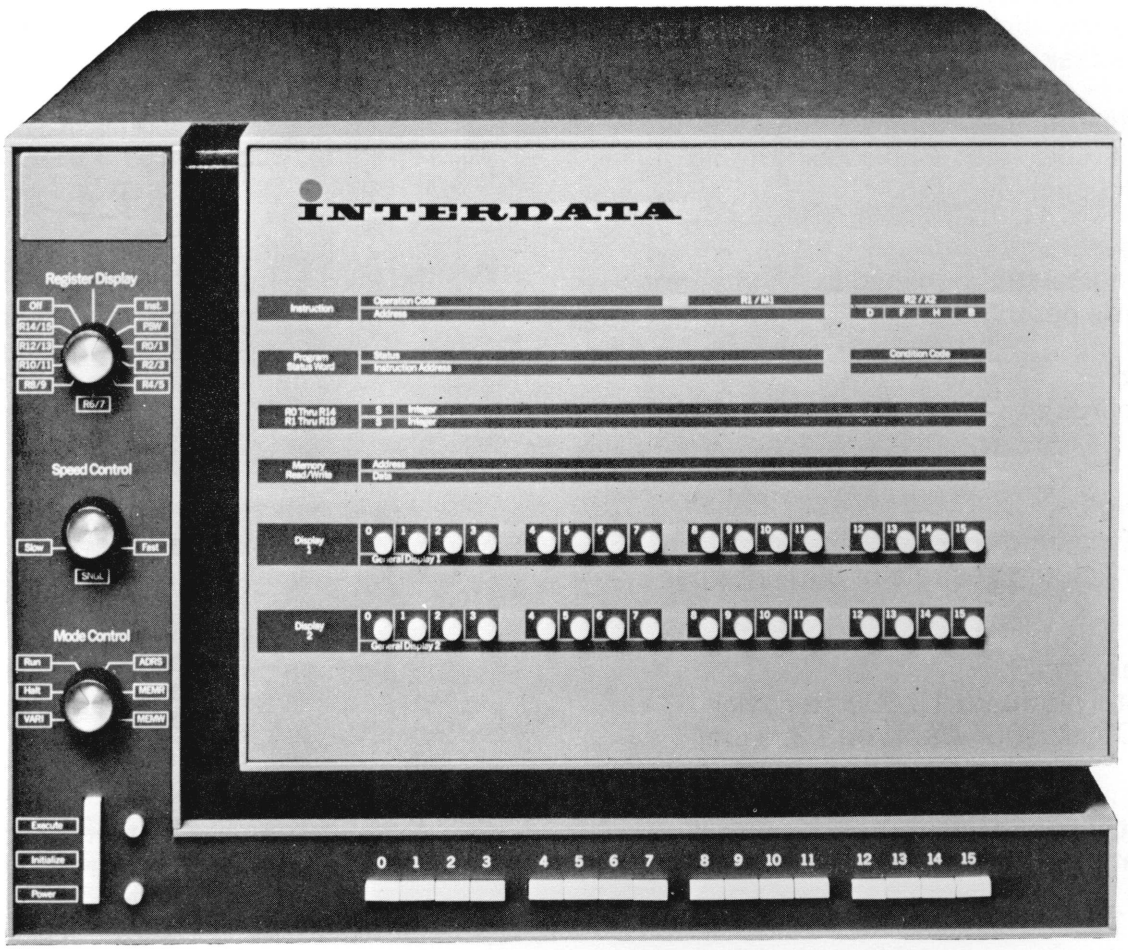
- ASR 33/35
- Card Reader
- High Speed Paper Tape Reader
- High Speed Paper Tape Punch
- Line Printer
- Real Time Clock
- A-D, D-A Converters
- Relay Closure Module
- DVM

Media Conversion Utility routines:

- Tape to Printer
- Card to Printer

Console panel designed for efficient program checking.

A display panel for all models permits static or dynamic inspection of the general registers, program status register and instruction register. Dynamic display is under variable speed control or single step mode.



A full line of peripheral devices is available from Interdata.

Teletype.
Includes a keyboard, printer, paper tape reader and punch. Either the ASR 33 or the heavy duty ASR or KSR 35 can be provided.

IBM Selectric Typewriter.
Keyboard input; prints 15 cps.

Paper Tape Reader.
Reads 300 cps, eight level code, fan-fold tape. Mounts on desk top or rack panel.

Paper Tape Punch.
Punches 60 cps, eight level code, fan-fold tape. Rack panel mounted.

Card Reader.
Reads standard IBM punched cards at a rate of 200 cards per minute.

Card Punch.
Punches cards at a rate of 100 cards per minute.

Line Printer.
Prints 128 columns per line with 64 characters per column at a rate of 300 lines per minute.

X-Y Plotter.
Incremental plotter at 18,000 steps per minute, .01 or .005″ steps, on 12″ wide paper.

X-Y Oscilloscope Display.
Plots point to point, 10 bits/axis.

Magnetic Tape.
High speed or incremental transport systems with either 7 or 9 track IBM compatible tape.

Disc Storage.
Disc system with up to 700K bytes of storage and transfer rates up to 500K bytes per second.

Data Communication Terminals.
Provide connection to the telephone system via standard data sets.

Conversion Equipment.
Analog to digital and digital to analog converters; 8, 10 or 12 bits including sign with multi-channel input/output optional.

System modules to meet virtually all requirements.

Interfaces to connect a broad range of application-oriented devices are available through standard Interdata system modules. Frequently required input-output and control function modules as well as conversion equipment are packaged as plug-in cards for easy connection to user systems. Some standard Interdata system modules are:

A Byte I/O Module supplies a completely buffered interface for byte-oriented devices and provides 8 data input lines, 8 data output lines plus 8 control lines, 8 sense lines and a priority interrupt line.

The Halfword I/O Module is similar except that 16 input and output data lines are supplied.

A Sense Line Module contains 16 sense lines which may be used for detecting the status of devices under external control.

The Control Line Module provides 16 buffered control lines for activation of up to sixteen external drives.

The Relay Closure Module has 16 isolated reed relay closures with storage registers for operation of medium power external devices.

Other units available include sense switches, manual data entry, decimal display indicators, and group priority interrupt modules.

Logic Components for Special Interface

For special system interfacing requirements a compatible set of functional components are available. The family of components includes general logic, flip flops and counters, and clock and timing circuits.

Logic components are mounted on standard Interdata printed circuit 'daughter' boards which can be mounted on larger 'mother' boards and interconnected by wire-wrap terminators. The larger boards are plugged into an expansion chassis having its back panel prewired for the multiplexor bus interface. Connection to external equipment is made by functional cable boards mounted on a specified field of the mother board.

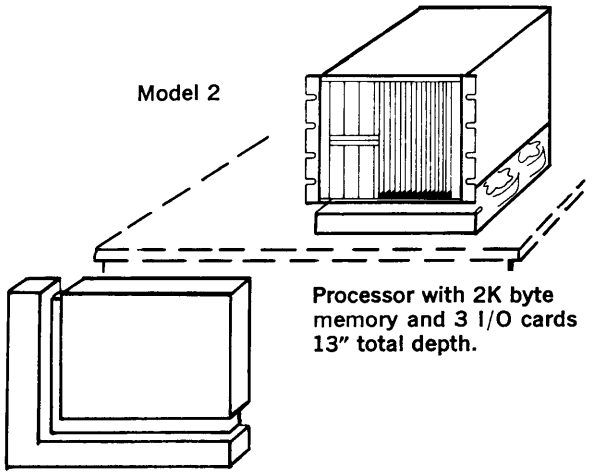
Interdata Provides Complete Training and Service Facilities.

Interdata schedules frequent programming and maintenance courses for purchasers of its computing systems. An experienced staff of instructors gives individual attention and guidance in all phases of programming, equipment operation and maintenance. Equipment is made available to the student to insure understanding of the system.

Regional centers provide local access to equipment, technical assistance, and twenty-four hour "on-call" service. Each center is staffed by qualified and experienced personnel to provide customer service on an individual need basis. Interdata extends a 90 day parts warranty and a selection of installation and service contracts to meet user needs.

Interdata systems are compact, fit in rack or on desk.

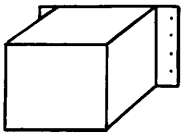
Model 2



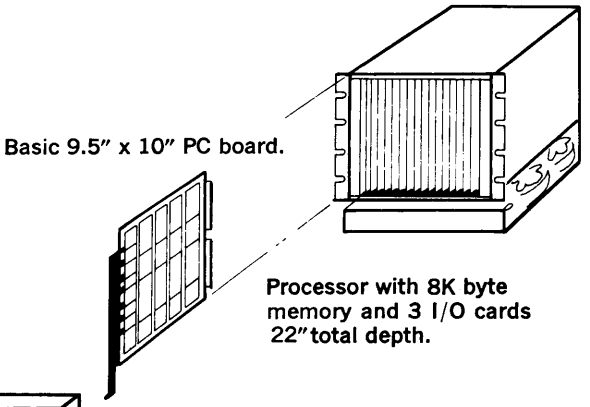
Processor with 2K byte memory and 3 I/O cards 13" total depth.

Front display panel (detachable)

Model 3

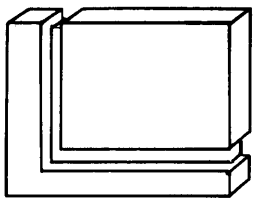


Power supply hinges out for access to back panel wiring.



Basic 9.5" x 10" PC board.

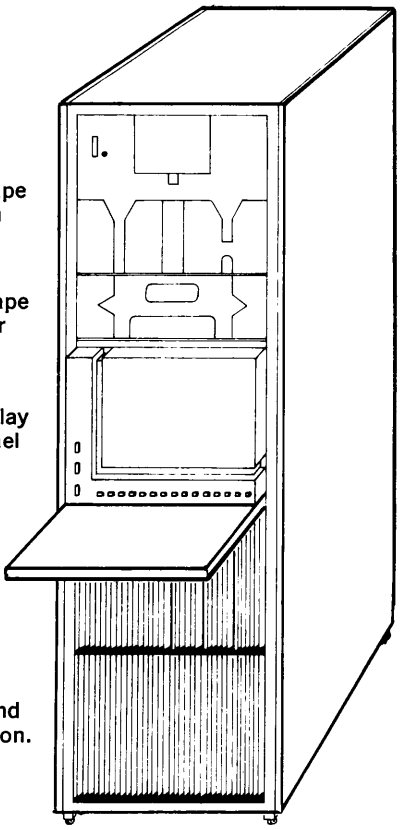
Processor with 8K byte memory and 3 I/O cards 22"total depth.



19"

13.97"

Model 4



Paper tape punch

Paper tape reader

Display panel

Processor with 8K byte memory and 2 I/O cards

Memory and I/O expansion.

24" total depth, 66" high.

Select the system to fit your application

Feature	Model 2	Model 3	Model 4
Memory:			
Cycle time	3 μs	1.8 μs	1.5 μs
Minimum/maximum byte capacity	1K–2K	4K–64K	4K–64K
Instruction repertoire and timing:			
Add time (RR format)	45 μs	34 μs	3.9 μs
General Registers and PSW	Core	Core	Hardware
Hardware multiply/ divide option	No	Yes	Yes
Hardware floating point option	No	No	Yes
Input/output:			
Priority interrupt system, 256 devices	Yes	Yes	Yes
Hardware block transfer option	No	Yes	Yes
High speed memory access options	No	Yes	Yes
Transfer Rates:			
Read/write data	5KBPS	6KBPS	20 KBPS
Read/write block	N.A.	100 KBPS	150 KBPS
Selector Channel	N.A.	500 KBPS	600 KBPS
Direct Memory Access	N.A.	750 KBPS	900 KBPS
Read-increment Write 16-bit halfword	N.A.	250KC	300KC
Software:			
FORTRAN	No	Yes	Yes
Assembler	No	Yes	Yes
Debug	Yes	Yes	Yes
Editor	Yes	Yes	Yes
Math Library	Yes	Yes	Yes
Input/output system	Yes	Yes	Yes

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